CLAIMS

What is claimed is:

1. A method for fabricating a semiconductor package, comprising the steps of:

preparing a substrate mounted with at least one semiconductor chip thereon via a plurality of conductive elements;

providing a mold having a molding cavity dimensioned to accommodate the semiconductor chip therein, wherein the molding cavity is formed with a plurality of recess portions, which are dimensioned to be relatively smaller in height than the molding cavity, and the recess portions are each connected to an air vent formed in the mold for interconnecting the recess portions and outside of the mold; and

placing the substrate with the semiconductor chip mounted thereon in the mold, and injecting a molding compound into the molding cavity to encapsulate the semiconductor chip.

2. The method of claim 1, wherein the semiconductor package is a BGA (ball grid array) semiconductor package.
3. The method of claim 1, wherein the semiconductor package is a FCBGA (flip chip ball grid array) semiconductor package.
4. The method of claim 1, wherein the conductive elements are solder bumps.
5. The method of claim 1, wherein the conductive elements are gold wires.
6. The method of claim 1, wherein the molding compound is an epoxy resin having low viscosity, high fluidity and small fine filler size.
7. The method of claim 1, wherein a molded underfilling technique is employed for injecting the molding compound.
8. A semiconductor package, comprising:

a substrate mounted with at least one semiconductor chip thereon and electrically connected to the semiconductor chip; and

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an encapsulant formed by a molding compound injected into a molding cavity of a mold for encapsulating the semiconductor chip mounted on the substrate, wherein the molding cavity is formed with a plurality of recess portions, which are dimensioned to be relatively smaller in height than the molding cavity, and the recess portions are each connected to an air vent formed in the mold for interconnecting the recess portions and outside of the mold.

9. The semiconductor package of claim 8, wherein the semiconductor package is a BGA (ball grid array) semiconductor package.

10. The semiconductor package of claim 8, wherein the semiconductor package is a FCBGA (flip chip ball grid array) semiconductor package.

11. The semiconductor package of claim 8, wherein the molding compound is an epoxy resin having low viscosity, high fluidity and small fine filler size.

12. The semiconductor package of claim 8, wherein a molded underfilling technique is employed for injecting the molding compound.